Electronic Version
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Claims

[c1] 1. A semiconductor device comprising:

a first interconnect adjacent a second interconnect on an interconnect level;

spacers formed along adjacent sides of the first and second interconnects; and

an air gap formed between the first and second interconnects, the air gap extending above an upper surface of at least one of the first and second interconnects and below a lower surface of at least one of the first and second interconnects, distance between the spacers defining the width of the air gap.

[c2] 2. The semiconductor device of claim 1 wherein the air gap is self-aligned to the adjacent sides of the first and second interconnects.

[c3] 3. The semiconductor device of claim 1 wherein the spacers adjacent the sides of the first and second interconnects comprise silicon dioxide or silicon nitride.

[c4] 4. The semiconductor device of claim 1 further including, beneath the at least one of the first and second interconnects, an etch stop layer positioned over an underly-

ing via insulator level, and wherein the air gap extends below the lower surface of the at least one of the first and second interconnects by a distance corresponding to a thickness of the etch stop layer.

[c5] 5. The semiconductor device of claim 4 wherein the etch stop layer comprises silicon carbide.

[c6] 6. The semiconductor device of claim 4 wherein the underlying via insulator level comprises silicon dioxide or fluorinated silicon dioxide.

[c7] 7. The semiconductor device of claim 1 further including hardmask spacers self-aligned to either side of an upper portion of the air gap.

[c8] 8. The semiconductor device of claim 7 wherein the hardmask spacers comprise silicon dioxide or silicon nitride.

[c9] 9. The semiconductor device of claim 1 further including at least one insulative layer above the interconnect level and the air gap, and wherein the air gap extends into the insulative layer.

[c10] 10. The semiconductor device of claim 9 wherein the at least one insulative layer above the interconnect level and the air gap comprises silicon nitride or silicon car-

bon nitride as a capping layer for the interconnect and silicon dioxide or fluorinated silicon dioxide as an insulative layer above the capping layer.

[c11] 11. The semiconductor device of claim 1 further including hardmask spacers self-aligned to either side of an upper portion of the air gap, and an insulative layer above the interconnect level, the air gap and the hardmask spacers, and wherein the air gap extends between the hardmask spacers and upward into the insulative layer.

[c12] 12. The semiconductor device of claim 1, wherein the first and second interconnects are formed by a damascene or dual damascene process.

[c13] 13. The semiconductor device of claim 1, wherein the first and second interconnects comprise copper, aluminum, tungsten or gold.

[c14] 14. The semiconductor device of claim 1 further including, beneath one of the first and second interconnects, an etch stop layer positioned over at least one underlying via insulator level, and below the underlying via insulator, a second interconnect level.

[c15] 15. The semiconductor device of claim 14 further including, between the at least one underlying via insulator

level and the second interconnect level, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer.

[c16] 16. The semiconductor device of claim 1 further including, over each of the first and second interconnects, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer.

[c17] 17. A method for forming an air gap between a pair of interconnects on an interconnect level of a semiconductor device comprising:

depositing a plurality of insulative layers of a semiconductor device;

depositing a first hardmask insulative layer over the plurality of insulative layers;

removing portions of the first hardmask insulative layer to expose regions of the uppermost of the plurality of insulative layers over which interconnects are to be formed, the regions of over which interconnects are to be formed being spaced apart;

depositing a second hardmask insulator layer over the first hardmask layer and exposed regions of the uppermost of the plurality of insulative layers;

removing portions of the second hardmask insulative layer over the first hardmask insulative layer to ex-

pose regions of the uppermost of the plurality of insulative layers over which interconnects are to be formed, leaving second hardmask spacers adjacent to the regions of the uppermost of the plurality of insulative layers over which interconnects are to be formed;

using the first hardmask insulative layer and second hardmask spacers to etch the at least one of the underlying plurality of insulative layers to form interconnect openings;

depositing a conformal insulative layer to form spacers on sidewalls of the interconnect openings;

depositing conductive metal adjacent the conformal insulative layer spacers to form interconnects in the interconnect openings;

etching portions of the first hardmask insulative layer and underlying plurality of insulative layers between the interconnects and conformal insulative layer spacers, and leaving second hardmask spacers adjacent to the interconnects and conformal insulative layer spacers, to form an air gap extending below at least one of the interconnects;

depositing at least one insulative layer over the air gap and over the interconnects and conformal insulative layer spacers to seal the air gap.

[c18] 18. The method of claim 17 wherein the air gap extends above the interconnects, into the at least one insulative layer.

[c19] 19. The method of claim 17 wherein the step of depositing a plurality of insulative layers of a semiconductor device comprises depositing a first insulative capping layer of a semiconductor device; depositing a second insulative layer over the first insulative capping layer; depositing a third insulative layer etch stop layer over the second insulative layer; and depositing a fourth insulative layer over the third insulative etch stop layer;

wherein removing portions of the first hardmask insulative layer exposes regions of the fourth insulative layer over which the interconnects are to be formed; and

wherein there are etched portions of the first hardmask insulative layer, fourth insulative layer and third insulative etch stop layer between the interconnects and conformal insulative layer spacers, to leave the second hardmask spacers adjacent to the interconnects and conformal insulative layer spacers, and to form the air gap extending below at least one of the interconnects.

[c20] 20. The method of claim 19 wherein the at least one insulative layer over the interconnects comprises a fifth in-

sulative capping layer for the interconnect and a sixth insulative layer above the capping layer, and wherein the air gap extends completely through the fifth capping layer and into a portion of the sixth insulative layer.